LEADFRAME TYPE SEMICONDUCTOR PACKAGE HAVING REDUCED INDUCTANCE AND ITS MANUFACTURING METHOD

INVENTORS

Gi Jeong Kim

Jin Han Kim

Jin Seok Oh

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] Not Applicable

STATEMENT RE: FEDERALLY SPONSORED RESEARCH/DEVELOPMENT

[0002] Not Applicable

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0003] The present invention relates generally to semiconductor packages, and more particularly to a semiconductor package having reduced inductance, and a method of manufacturing such semiconductor package.

2. Description of the Related Art

[0004] Semiconductor dies are conventionally enclosed in plastic packages that provide protection from hostile environments and enable electrical interconnection between the semiconductor die and an underlying substrate such as a printed circuit board (PCB) or motherboard. The elements of such a package include a metal leadframe, an integrated circuit or semiconductor die, bonding material to attach the semiconductor die to the leadframe, bond wires which electrically connect pads or terminals on the semiconductor die to individual leads of the leadframe, and a hard plastic encapsulant material which covers the other components and forms the exterior of the semiconductor package commonly referred to as the package body.

[0005] The leadframe is the central supporting structure of a semiconductor package. In many semiconductor package designs, that portion of the leadframe to which the semiconductor die is bonded effectively functions as and is commonly referred to as a heat sink. In most semiconductor package configurations, a portion of the leadframe is internal to the package, (i.e., completely surrounded by the package body). Portions of the leads of the leadframe typically extend externally from the package body or are partially exposed therein for use in electrically connecting the package to another component. Similarly, at least a portion of the heat sink is exposed in the package body to discharge heat generated by the semiconductor die. The heat sink of the leadframe is also often referred to as a die pad.

[0006] In the electronics industry, there is continued development of semiconductor dies which have increasing processing speeds and higher degrees of integration. For a semiconductor package to accommodate these enhanced semiconductor dies, the number of leads included in the semiconductor package must be significantly increased. To avoid an undesirable increase in the size of the semiconductor package attributable to the increased number of leads, a common practice is to reduce or narrow the lead pitch. However, a result of the narrowing of the lead pitch is an increase in the level of self inductance and mutual inductance (hereinafter collectively referred to as "inductance") generated from the leads of the semiconductor package. Thus, leadframe type semiconductor packages are typically considered to be unsuitable for semiconductor dies which transmit signals at high speed since the relatively high inductance of such semiconductor packages may distort the signals transmitted from such high speed semiconductor dies. In this regard, many mobile communication devices (e.g., cellular phones) and personal communication devices which are equipped with semiconductor dies capable of transmitting high-frequency signals typically are outfitted with BGA (ball grid array) semiconductor packages which accommodate such semiconductor dies. If such semiconductor dies were to be installed or packaged in a leadframe type semiconductor package, significant signal loss may be created due to the inductance problem described above.

[0007] In recognition of this problem and the need to change the structure of leadframe type semiconductor packages to accommodate semiconductor dies which transmit signals at high speeds, there has been developed in the prior art a leadframe type semiconductor package wherein a semiconductor die and a ground lead are each bonded to a heat sink or die pad through the use of conductive wires, thereby reducing inductance with respect to the ground lead.

However, the effective reduction in inductance achieved in this type of semiconductor package is not significant since only a narrow area of the heat sink or die pad bonded to the conductive wire acts a ground, with the remaining area of the heat sink or die pad not acting as a ground. These deficiencies are addressed and overcome by the semiconductor package constructed in accordance with the present invention, as will be described in more detail below.

BRIEF SUMMARY OF THE INVENTION

[0008] In accordance with the present invention, there is provided a leadframe type semiconductor package which is specifically configured to provide significant inductance reduction when used to accommodate a semiconductor die capable of transmitting high-frequency signals at high speed. To facilitate such inductance reduction, the leadframe of the semiconductor package of the present invention includes first and second ground leads which are attached to the top surface of a heat sink and segregated into pairs. The first and second ground leads of each pair are arranged in aligned, spaced relation to each other, and are disposed between a corresponding adjacent pair of the signal or power leads of the semiconductor package. The semiconductor die, the first and second ground leads of each pair, and the heat sink are conductively connected to each other through the use of multiple ground wires. Thus, in the semiconductor package of the present invention, the heat sink rapidly discharges heat generated from the semiconductor die, while acting as an enlarged ground area, thus reducing package inductance and improving the electrical performance of the semiconductor die.

[0009] The present invention is best understood by reference to the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] These, as well as other features of the present invention, will become more apparent upon reference to the drawings wherein:

[0011] Figure 1A is a cross-sectional view of a semiconductor package constructed in accordance with a first embodiment of the present invention;

[0012] Figure 1B is a partial perspective view of the semiconductor package shown in Figure 1A, with a portion of the package body of the semiconductor package being removed;

[0013] Figure 1C is a top perspective view of the heat sink of the semiconductor package shown in Figure 1A;

[0014] Figure 2 is a cross-sectional view of a semiconductor package constructed in accordance with a second embodiment of the present invention; and

[0015] Figures 3A-3E illustrate an exemplary sequence of steps which may be used to facilitate the fabrication of the semiconductor package of the first embodiment shown in Figures 1A-1C.

[0016] Common reference numerals are used throughout the drawings and detailed description to indicate like elements.

DETAILED DESCRIPTION OF THE INVENTION

[0017] Referring now to the drawings wherein the showings are for purposes of illustrating preferred embodiments of the present application only, and not for purposes of limiting the same, Figures 1A-1C illustrate a semiconductor package 100 constructed in accordance with a first embodiment of the present invention. The semiconductor package 100 comprises a leadframe having a die pad or heat sink 110. The heat sink 110 includes a generally planar first (top) surface 111 and an opposed, generally planar second (bottom) surface 112. As best seen in Figures 1A and 1C, the area of the top surface 111 exceeds that of the bottom surface 112. In this regard, the heat sink 110 defines a continuous shelf which is disposed in opposed relation to the top surface 111 and circumvents the bottom surface 112. More particularly, the shelf is perpendicularly recessed relative to the bottom surface 112. The recessed shelf is used to increase the bonding or adhesion force between the package body of the semiconductor package 100 and the heat sink 110, as will be discussed in more detail below. The heat sink 110 preferably has a generally quadrangular shape (e.g., square) defining four sides or peripheral edge segments, and hence four corner regions.

[0018] As seen in Figures 1A-1C, disposed on the top surface 111 of the heat sink 110 is a plating section 113. The plating section 113 includes a first plating region 113a which has a ring-like shape and is disposed in the central portion of the top surface 111 of the heat sink 110. In addition to the first region 113a, the plating section 113 includes a plurality of second regions 113b which are integrally connected to and extend linearly or radially from the first section 113a. The distal ends of the second regions 113b are integrally connected to a continuous third region

113c of the plating section 113. As best seen in Figure 1C, the third region 113c of the plating section 113 extends along and in close proximity to the peripheral edge of the top surface 111 of the heat sink 110. In the plating section 113, the second regions 113b improve a skin effect, i.e., a surface electronic mobility between the first region 113a and the third region 113c.

[0019] In the semiconductor package 100, it is contemplated that the heat sink 110 of the leadframe will be made of copper, aluminum, or a similar material. However, those of ordinary skill in the art will recognize that the present invention is not limited to any particular material for the heat sink 110, or the specific shapes of the first and third plating regions 113a, 113c as shown in Figure 1C. Nor is the present invention limited to the specific number of second regions 113b shown in Figure 1C. It is further contemplated that the plating section 113 will be fabricated from the application of silver or a similar, suitable conductive material to the top surface 111 of the heat sink 110.

[0020] In the semiconductor package 100, a semiconductor die 120 is bonded to the top surface 111 of the heat sink 110 within the first region 113a of the plating section 113, i.e., the first region 113a circumvents the semiconductor die 120. The attachment of the semiconductor die 120 to the top surface 111 of the heat sink 110 is preferably accomplished through the use of a layer 124 of a suitable adhesive. Included on the upper surface of the semiconductor die 120 is a plurality of terminals or bond pads 122.

[0021] In addition to the heat sink 110, the leadframe of the semiconductor package 100 includes at least one first ground lead 130 which is bonded to the top surface 111 of the heat sink 110. The attachment of the first ground lead 130 to the top surface 111 is preferably facilitated by a first insulating layer 150. As best seen in Figure 1A, the first ground lead 130 is positioned, in its entirety, inwardly of the peripheral edge of the top surface 111, i.e., no portion of the first ground lead 130 protrudes beyond the peripheral edge of the top surface 111. It is contemplated that the first insulating layer 150 used to secure the first ground lead 130 to the top surface 111 may be positioned above one of the second regions 113b of the plating section 113.

[0022] In addition to the first ground lead 130, the leadframe of the semiconductor package 100 includes at least one second ground lead 140 which, like the first ground lead 130, is also bonded to the top surface 111 of the heat sink 110. The attachment of the second ground lead 140 to the top surface 111 is preferably facilitated by a second insulating layer 160. However, the length of the second ground lead 140 substantially exceeds that of the first ground lead 130,

with only an inner end portion of the second ground lead 140 extending to the inner end thereof being positioned over the top surface 111 of the heat sink 110. In this regard, as is best seen in Figure 1A, the majority of the length of the second ground lead 140 protrudes outwardly beyond the peripheral edge 111 of the heat sink 110. As is best seen in Figure 1B, the first and second ground leads 130, 140 are preferably oriented relative to each other such that the outer end of the first ground lead 130, (i.e., the end disposed furthest from the semiconductor die 120) is located in close proximity to, but spaced from the inner end of the second ground lead 140, the first and second ground leads 130, 140 extending in substantially aligned relation to each other. The first and second ground leads 130, 140 are also oriented relative to the plating section 113 such that the third region 113c extends in the gap defined between the outer end of the first ground lead 130 and the inner end of the second ground lead 140, in the manner best shown in Figure 1A. It is contemplated that a portion of one second region 113b of the plating section 113 and/or a portion of the third region 113c of the plating section 113 may be positioned below the second insulating layer 160 used to attach the second ground lead 140 to the heat sink 110.

[0023] The first and second insulating layers 150, 160 described above preferably each comprise a segment of a polyimide tape. However, those of ordinary skill in the art will recognize that the present invention is not limited to any particular material for the first and second insulating layers 150, 160. Additionally, it is contemplated that the first and second ground leads 130, 140 will each be fabricated from copper, a copper alloy, or another suitable conductive material, though the present invention is not limited to any particular material for the first and second ground leads 130, 140.

[0024] In addition to the first and second ground leads 130, 140, the leadframe of the semiconductor package 100 comprises a plurality of signal leads (or power leads) 175. The signal leads 175 extend in spaced relation to each other, and are preferably arranged to circumvent the semiconductor die 120. As best seen in Figure 1B, the aligned first and second ground leads 130, 140 extend between an adjacent pair of the signal leads 175. Though only one aligned pair of first and second ground leads 130, 140 is shown in Figure 1B, those of ordinary skill in the art will recognize that the leadframe of the semiconductor package 100 may be outfitted with additional aligned pairs of first and second ground leads 130, 140 which are located between other adjacent pairs of the signal leads 175 in the leadframe. It is further contemplated that the leadframe of the semiconductor package 100 may also include a ground

ring or a power ring 176 which is positioned between the semiconductor die 120 and the first ground lead 130. Assuming that multiple pairs of the first and second ground leads 130, 140 are included in the leadframe, it is contemplated that the ring 176 will be positioned on the first insulating layers 150 used to attach the first ground leads 130 to the top surface 111, in the manner shown in Figure 1A.

[0025] In the semiconductor package 100, a first pair of ground wires 170 and a second pair of ground wires 180 is used to facilitate desired conductive connections between the semiconductor die 120, plating section 113, and first and second ground leads 130, 140. More particularly, as seen in Figures 1A and 1B, a first ground wire 170 of the first set is used to connect one of the bond pads 122 of the semiconductor die 120 to the first region 113a of the plating section 113, with a second ground wire 170 of the first set being used to connect the first region 113a to the first ground lead 130. Thus, the ground wires 170 of the first set effectively connect the semiconductor die 120 to the first ground lead 130 via the first region 113a of the plating section 113. Thus, a ground signal of the semiconductor die 120 is transferred or transmitted to the first ground lead 130 by way of the ground wires 170 and heat sink 110.

[0026] As is further seen in Figures 1A and 1B, a first ground wire 180 of the second set is used to connect the first ground lead 130 to the third region 113c of the plating section 113. A second ground wire 180 of the second set is used to connect the second ground lead 140 to the third region 113c of the plating section 113. Thus, the ground signal generated from the semiconductor 120, in addition to being transferred to the first ground lead 130, is also transferred or transmitted to the second ground lead 140. That is, the ground signal of the semiconductor die 120 is transferred to the heat sink 110 and the first ground lead 130 through the ground wires 170 of the first set, and is transferred to the second ground lead 140 through the ground wires 180 of the second set. Further, the ground signal transferred to the first region 113a of the heat sink 110 is transferred to the third region 113c via the second regions 113b and is thus transferred to the second ground lead 140 by the ground wire 180 which extends from the third region 113c to the second ground lead 140.

[0027] Based on the foregoing, the ground signal of the semiconductor die 120 is transferred to an external device by way of the ground wires 170 of the first set, the first ground lead 130, the ground wires 180 of the second set, and the second ground lead 140. However, the ground signal of the semiconductor die 120 can also be transferred to the external device through the

heat sink 110 which is overlapped with the first ground lead 130, the first region 113a, the second region 113b, and the third region 113c. Accordingly, both the first ground lead 130 and heat sink 110 can be used as a ground plane, thereby increasing ground effect. Thus, in accordance with the present invention, inductance of the leads 175 positioned adjacent to the first ground lead 130 is significantly reduced. The reason for such significant reduction is that not only is the ground signal transferred to the second ground lead 140 through the ground wires 170 of the first set, the first ground lead 130, and the ground wires 180 of the second set, but is also transferred to the first, second and third plating regions 113a, 113b, 113c and the second ground lead 140 by one of the ground wires 170 and one of the ground wires 180. The ground wires 170, 180 of the first and second sets may be fabricated from gold, aluminum, copper or similar conductive materials, though the present invention is not limited to any particular material for the first and second ground wires 170, 180.

[0028] It is contemplated that in the semiconductor package 100, the ground wire 170 extending between the first ground lead 130 and first region 113a can be omitted. Similarly, the ground wire 180 of the second set extending between the first ground lead 130 and third region 113c can be omitted.

[0029] The semiconductor package 100 of the first embodiment further comprises a package body 190 which at least partially covers or encapsulates the heat sink 110, the semiconductor die 120, the first and second ground leads 130, 140, the first and second ground wires 170, 180 and the signal leads 175. However, as is seen in Figure 1A, substantial portions of the second ground leads 140 and signal leads 175 protrude from the side surface of the package body 190, so as to be easily connectible to an external device. In addition, the thickness of the heat sink 110 is substantially greater than the thickness of each of the first and second ground leads 130, 140, so that the bottom surface 112 of the heat sink 110 is exposed in and substantially flush with a bottom exterior surface of the package body 190. Thus, heat generated by the semiconductor die 120 and the leads 175 may be easily discharged to the exterior of the semiconductor package 100 through the heat sink 110. Thus, in the semiconductor package 100, the hest sink 110 rapidly discharges heat generated from the semiconductor die 120 while acting an enlarged ground area, thus reducing package inductance and improving the electrical performance of the semiconductor die 120. The covering of the recessed shelf of the heat sink 110 with the package body 190 effectively locks the heat sink 110 to the package body 190.

[0030] Referring now to Figures 3A-3E, there is shown an exemplary sequence of steps which may be used to facilitate the fabrication of the semiconductor package 100 of the first embodiment of the present invention. The initial step of the fabrication method comprises providing the heat sink 110 having the above-described structural attributes and including the above-described plating section 113 applied to the top surface 111 (Figure 3A). Thereafter, multiple first ground leads 130 and multiple second ground leads 140 are bonded to the top surface 111 of the heat sink 110 through the use of the first and second insulating layers 150, 160 in the above-described orientations (Figure 3B). As indicated above, the first and second ground leads 130, 140 are oriented relative to the plating section 113 such that the first region 113a is disposed inward of the inner ends of the first ground leads 130, with the third region 113c extending and being exposed between the outer ends of the first ground leads 130 and the inner ends of the second ground leads 140. It is contemplated that each pair of first and second ground leads 130, 140 may be formed by initially bonding a single lead to the top surface 111 of the heat sink 110, and thereafter punch-cutting such lead in a manner effectively forming the separate first and second ground leads 130, 140. A portion of the single insulating layer which would be used to attach such single lead to the top surface 111 would also be removed such that the third region 113c of the plating section 113 is exposed between the first and second ground leads 130, 140 formed by the cutting of the single lead as described above. At the time each pair of first and second ground leads 130, 140 is attached to the heat sink 110 in the above-described manner, such pairs of first and second ground leads 130, 140 are already positioned between adjacent pairs of the leads 175, though such leads 175 are not shown in Figure 3B. However, the above-described ring 176 of the leadframe of the semiconductor package 100 which is actually integrally connected to certain ones of the leads 175 as shown in Figure 1B is depicted in Figure 3B. Thus, at the time each pair of first and second ground leads 130, 140 is attached to the heat sink 110, the leads 175 and ring 176 (if included in the leadframe) are also cooperatively interfaced to the heat sink 110 in the above-described orientations.

[0031] In the next step of the preferred assembly method, the semiconductor die is bonded to the top surface 111 of the heat sink 110 within the first region 113a through the use of the adhesive layer 124 (Figure 3C). It is not necessarily required to locate the semiconductor die 120 in the center of the heat sink 110 within the first region 113a of the plating section 113. In

this regard, a portion of the semiconductor die 120 may be positioned over a portion of the first region 113a.

[0032] Subsequent to the attachment of the semiconductor die 120 to the heat sink 110, the ground wires 170, 180 are extended between bond pads 122 of the semiconductor die 120, the plating section 113, and the first and second ground leads 130, 140 of each pair in the above-described manner so as to facilitate the desired pattern of conductive connections between such components (Figure 3D). This pattern of conductive connections provides the inductance reduction advantages described above. During the process of adding the first and second ground wires 170, 180 to the semiconductor package 100, other bond pads 122 of the semiconductor die 120 are wire-bonded to the leads 175.

[0033] Subsequent to the conductive connection of the semiconductor die 120 to the leads 175 and first and second ground leads 130, 140 of each pair in the above-described manner, an encapsulant material is applied to the semiconductor die 120, heat sink 110, first and second ground leads 130, 140 of each pair, the first and second ground wires 170, 180 and leads 175, as well as the wire bonds extending between the semiconductor die 120 and leads 175 (Figure 3E). The hardening of the encapsulant material facilitates the formation of the package body 190 of the semiconductor package 100. In the fully formed semiconductor package 100, the bottom surface 112 of the heat sink 110 is exposed in and substantially flush with the bottom exterior surface of the package body 190.

[0034] Referring now to Figure 2, there is shown a semiconductor package 200 constructed in accordance with a second embodiment of the present invention. In Figure 2, the 200 series reference numerals are used to identify elements corresponding to those identified with the 100 series reference numerals in Figures 1A-1C. The major distinction between the semiconductor packages 100, 200 lies in the configuration of the heat sink 210 of the semiconductor package 200 in comparison to the heat sink 110 of the semiconductor package 100. More particularly, in the semiconductor package 200, the thickness of the heat sink 210 is substantially identical to or less than the thickness of each of the first and second ground leads 230, 240. In this regard, the heat sink 210 is made of a material identical to that of the first and second ground leads 230, 240, and is actually formed concurrently with the formation of the first and second ground leads 230, 240. Due to its reduced thickness, the heat sink 210 is completely covered by the package body 290, with no portion of the bottom surface 212 of the heat sink 210 being exposed in the package

body 290. Though the heat sink 210 does not dissipate heat in the same manner as does the heat sink 110, the heat sink 210 still functions to discharge heat to the exterior of the semiconductor package 200 through the first and second ground leads 230, 240 of each pair, as well as the signal leads or power leads of the semiconductor package 200. The heat sink 210 still acts as a ground plane when the semiconductor die 220 is operated, thereby reducing inductance. As will be recognized, the manufacturing method for the semiconductor package 200 is substantially the same as that described above in relation to the semiconductor package 100, except that the encapsulant material which hardens into the package body 290 is applied to the heat sink 210 in a manner completely covering the same such that no portion of the heat sink 210 is exposed in the package body 290.

[0035] This disclosure provides exemplary embodiments of the present invention. The scope of the present invention is not limited by these exemplary embodiments. Numerous variations, whether explicitly provided for by the specification or implied by the specification, such as variations in structure, dimension, type of material and manufacturing process, may be implemented by one of skill in the art in view of this disclosure.